5G -NR Open-Radio Unit (O-RU) Reference Design Platform

Get your radio design up and running quickly with reference design enablement

The Radio Access Network (RAN) is the most critical part of the new 5G networks. 5G aims to deliver more data, faster and with lower latency require a complete rethink on how the RAN is designed. It also requires a rethink on how the RAN is implemented. 5G RAN infrastructure total cost of ownership (TCO) can grow by 65% compared to the current 4G RAN costs. Energy costs can grow as much as 140%. Managing these costs is critical to the carrier business case.

Developing a 5G RAN that can meet future service needs cost-effectively is more than one carrier or the vendor can address on their own. Collaboration on the development of open, standards-based, virtualized solutions have become a necessity as carriers seek opportunities to reduce costs, while also enabling a more flexible, dynamic, and responsive RAN.

Intel®, Analog Devices Inc (ADI), and Whizz Systems have designed and built a 5G NR Open-Radio Unit (O-RU) which significantly reduces the cost of development while giving time to market advantage. The cutting-edge silicon namely Arria® 10 SoC FPGA from Intel® and ADRV9025 Quad-Transceiver from ADI offers the optimized BOM cost and power while offering industry-grade performance. Whizz Systems leverages this cutting-edge silicon and has built the reference design platform shown in Figure 1.
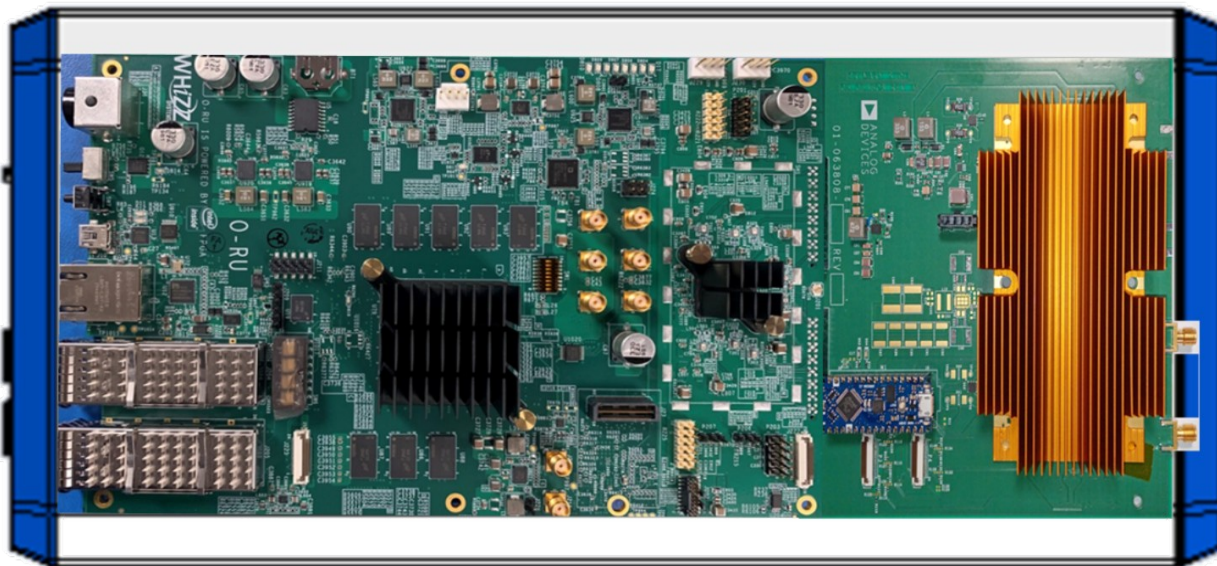

Figure 1 O-RU Reference Platform

This 5G reference design platform can support up to 4-Transmit 4-Receive (4T4R) paths in sub6GHz while supporting up to 3GPP split 7.2 functionality. The reference design platform is aligned to O-RAN Alliance reference designs are provided as "white-box" implementations specified in working group 7 (WG7).
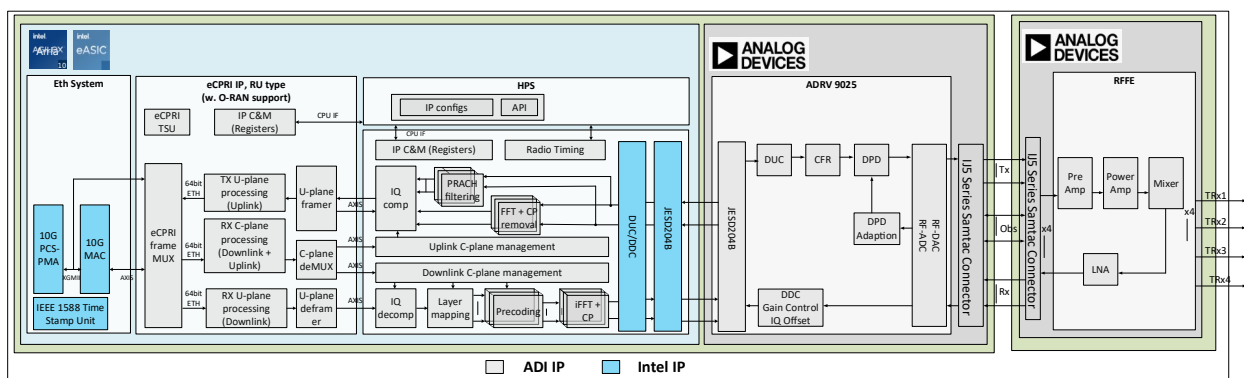
Solution Architecture

Figure 2 Solution Architecture

Figure 2 shows the solution architecture for the reference design platform. It contains blocks coming from Intel, ADI. Let's discuss each in brief.

The Intel® Arria® 10 SoC delivers optimal performance, power efficiency, small form factor, and low cost for midrange applications. The Intel Arria 10 SoC combines a dual-core ARM Cortex-A9 MPCore, Hard Processor System (HPS) with industry-leading programmable logic technology that includes hardened floating-point digital signal processing (DSP) blocks. The Intel Arria 10 SoC offers a processor with a rich feature set of embedded peripherals, hardened floating-point variable-precision DSP blocks, embedded high-speed transceivers, hard memory controllers, and protocol intellectual property (IP) controllers - all in a single highly integrated package.

The ADI 5G NR O-RAN IP is production-ready optimized goes in to Intel® Arria® 10 SoC FPGA as shown in figure. The solution is a resource-efficient implementation of the O-RAN standard optimized for the Intel® FPGA and ADI Transceiver, allowing easy reconfiguration of the functionality for various applications while still keeping an ultra-small footprint. IP elements consist of FIR, FFT/iFFT, CP adds/removal, Radio Timing, PRACH, Layer Mapping, IQ Compression/Decompression, O-RAN User Plane Framer/Deframer, Control Plane Mux/Demux, and FDD/TDD switching. The software environment runs on the Intel® FPGA HPS and integrates with O-DU with Intel FlexRAN reference SW.

The ADI ADRV9026 is their 4th generation wideband RF transceiver. It offers the smallest size reduces footprint and enhances form factor flexibility 2× integration and 50% power consumption reduction over ADRV9009 enables increased radiodensity to support higher antenna count Supports up to 200 MHz bandwidth and covers all bands from 650 MHz to 6 GHz Enables ORAN small cell designs with lowest system power and cost Single-chip FDD/TDD solution simplifies hardware and software development Common platform design for 3G/4G/5G reduces complexity, development costs and time to market.

The ADI RFFE Reference Design includes a circulator, directional coupler, power amplifier, drive amplifier, low noise amplifier, temp sensor, filter, and PA from an external vendor. The board supports heatsink and DC power synthesis as well as the microcontroller to ensure that the PA is biased properly for all operating conditions.

Solution Benefits

- ✓ Reference platform and ORAN IP available for evaluation & licensing
- ✓ Broader ecosystem availability for productization
- ✓ The platform can be repurposed for 2T2R, 2x2T2R, 4T4R across LTE, 5G, NB-IoT in Sub6GHz bands up to 200 MHz bandwidth
- ✓ Able to accommodate various indoor and outdoor scenario with 250mW to 60W PA
- ✓ Cutting edge silicon from Intel & ADI offers the lowest BOM & TCO benefits
- ✓ Unit cost and power reduction path through eASIC

Reference Design Platform Specification

The platform is targeted to accommodate a variety of use-cases across commercial, industrial, private, and fixed wireless access use-cases in Sub6GHz and up to 4T4R configurations. The detailed platform specifications are as follows:

Parameter	Value
RAT	3GPP LTT, 5G NR, NB-IoT
Antenna Channels	4 Transmit 4 Receive (4T4R)
RFFE	4x5W
Duplexing Mode	TDD / FDD
Frequency Range	600MHz – 6GHz
Max Signal Bandwidth	200MHz OBW
Protocols	ORAN Split 7.2/8 at 10GE link
FPGA	Intel Arria 10 SoC FPGA
Transceiver	ADRV9025
Clocking	AD9545 / ADCLK846
Synchronization	1588 v2 or CPRI recovered clock
Memory, Optical and data-rate	1GB DDR4 (HPS), 2GB DDR4 (FPGA Fabric for debug), EPCQ Flash,
Optical & Data-rate	SFP+ at 10GE or 9.8Gbps eCPRI
Connectors	2xQSFP+ Cage, RJ45, Clock I.O (SMA), IJ5 from Samtec
Dimension	8" x 8" (20.72cm x 20.72cm)

Learn More

You may find the following resources helpful:

- ADI ADRV9026 Integrated Quad RF Transceiver User Guide
- Intel Arria10 SoC FPGA User Guide
- Whizz System's 5G NR O-RU Reference Design Platform

For the solution that is right for your organization. Contact your Intel representative in your region or visit www.intel.com