5G Open Radio Unit White Box

Introduction

5G radio networks provide increased bandwidth at the expense of reduced range. To compensate for the reduced range and to increase coverage, the availability of cost effective radio units is critical. In collaboration with Intel, Analog Devices, Comcores, and Radisys, Whizz Systems has developed a 5G Open Radio Unit (ORU) white box solution to meet this market need. A broader overview of the 5G architecture can be found in the Comcores article [1] and Radisys Whitepaper [2].

This white paper provides an overview of the design and development process for the various hardware components that make up the 5G ORU white box. Whizz Systems is responsible for the electrical, thermal, mechanical engineering, and manufacturing aspects, as well as system validation and bring up of the turn key white box ORU solution. This includes the design of the individual PCBAs and the industrial design of the enclosure.

The hardware design leverages Intel's Arria 10 reference design as a starting point with power and clocking schemes revamped to meet the updated power and clocking requirement for the ORU platform. An additional JESD interface as communication pathway is added between the Intel's Arria 10 FPGA & Analog Devices (ADI) based chip "ADRV902X". A board to board (BTB) header is also added to mate with either the ADI designed Radio Frequency Front End (RFFE) Card or the Whizz designed ORU Adapter Card.

SI/PI simulations are carried out to guarantee that the design meets requirements of the 5G ORU. Design of the chassis and simulation of thermal characteristics of the board for heat sink and fan selection is done by the Mechanical team.

The 5G white box PCB is eventually fabricated at Whizz Systems and processed through the Whizz standard bring up process and inspections where the manufactured board is tested for

shorts, proper power on sequence and bring up of all interfaces. Finally, the software team is involved for validation of QSFP, DDR, Madura and other major sub-systems.
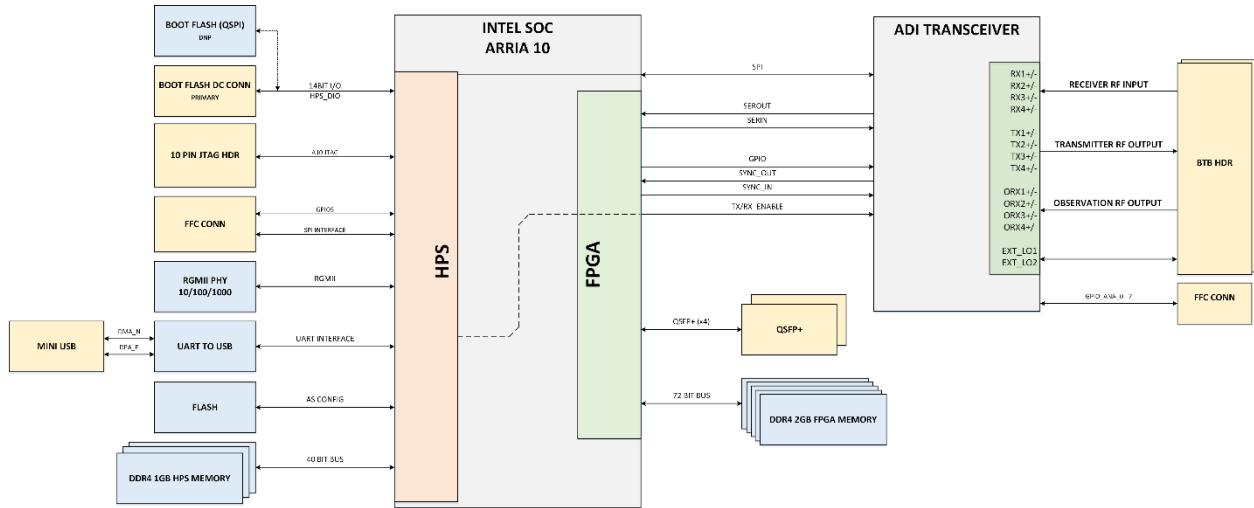
Hardware Electrical Specifications

Figure 1: System block diagram for the ORU card

The white box product consists of both the ORU PCBA and the RFFE PCBA but this white paper will mainly focus on ORU design. The ORU card is designed using low-power, high-performance and logic-intensive Intel's Arria® 10 SoC processor to create customized radio solutions with 4T4R TDD (Four Transmit and Four Receive Time Division Duplex) communication radio link having a tunable range of 600MHz to 6GHz, with a 100MHz signal bandwidth (oBW).

The White box ORU card design supports Intel's Arria® 10 SX 320/480 SoCs and has an on board 1GB DDR4 HPS Memory, 2GB DDR4 on-board FPGA memory as shown in Figure 1. The design also hosts a 1Gbps Ethernet interface, a USB to UART interface and two optical QSFP ports with each channel capable of 10Gbps with a total transfer rate of 40Gbps along with 1PPS/10MHz Clock for external synchronization. There exists two Warm/Cold Reset Push switches for the Intel Arria 10 on the faceplate along with a slide switch for power cutoff.

The Intel Arria 10 communicates with the QSFP ports using two SERDES banks, has a dedicated RGMII interfaces for the Ethernet port and uses a UART port for UART to USB conversion. HPS/FPGA banks are used for the HPS/FPGA Memories whereas JESD interface in form of SERDES is used to communicate with the ADI "ADRV902X" chip.

The user can use the on-board BTB Boot Flash connector to mount either an SD card module or a QSPI module as boot up options for the device. The board also hosts a total of three fan headers, eight user LEDs, an eight port SPST Dip-switch and six pin user IO connector.

The 5G White Box radio card also provides support for IJ5 Series Samtec Board to Board connector for external RFFE/Adapter board and another Board to Board connector for external SD card boot flash for Intel Arria 10 SoC. See Figure 2 for various components of the ORU PCBA.
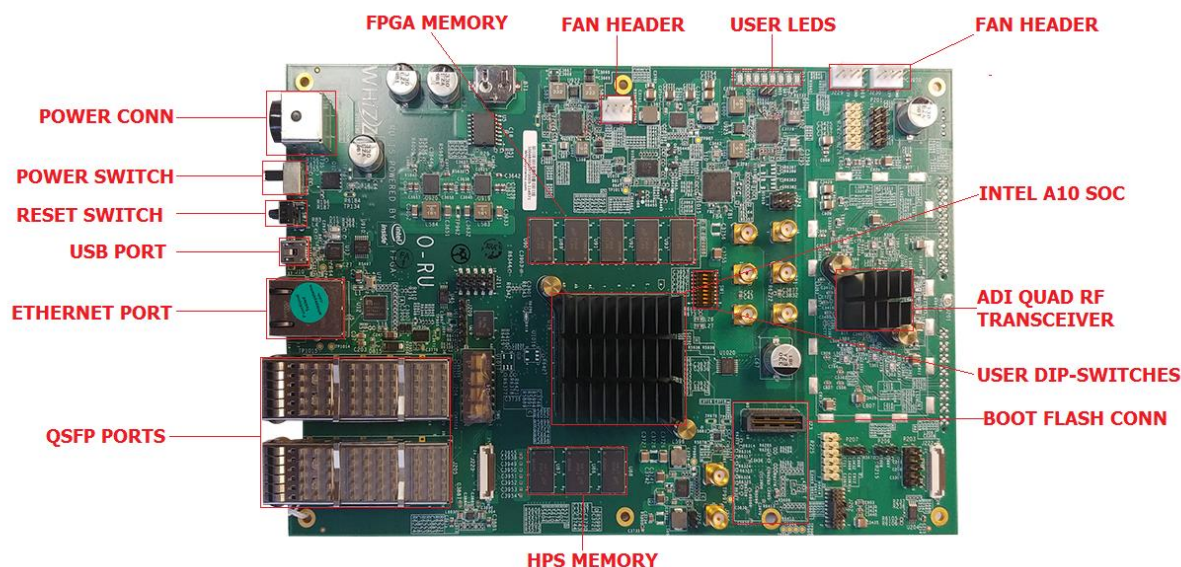
Figure 2: ORU PCBA

PCB Layout Design

PCB layout design is done considering the Electrical and Mechanical constraints for the application of the unit. Dielectric material selected is Isola 408HR because it's cost effective and the simulation/lab results of insertion loss for it are low enough for the required maximum speed of signals in design.

Several layout techniques are used for improved performance. For example, back-drilling is adopted to eliminate stubs, and separate Analog/Digital sections are employed to reduce noise and interference. Moreover, standard through hole via technology is used to reduce cost.

Reference planes are taken into consideration while routing high speed signal pairs. Less bends and optimized trace lengths are achieved to minimize the signal losses maintaining adequate space within traces and to all other features. Electrical Rules Check (ERC) and Design Rules Check (DRC) are run to ensure that all the established constraints are met.

Layout iterations are made based on analysis feedback such as thermal simulation enforced placement of power supplies and mechanical allowance for heat sinks. Connector placements and enclosure related changes are driven by 3D modeling of all sub-systems. SI/PI simulation recommendations are implemented for verification of optimum board functionality. Figure 3 shows both the RFFE and ORU cards.

Few challenges involved are making of special GND shield around ADI chip for RF signals isolation, FFC connector placement due to its connecting cable length constraint, power supply layout design due to complex copper pour shapes, implementation of special GSSG via pattern and plane voids for high speed signal integrity of QSFP signals.
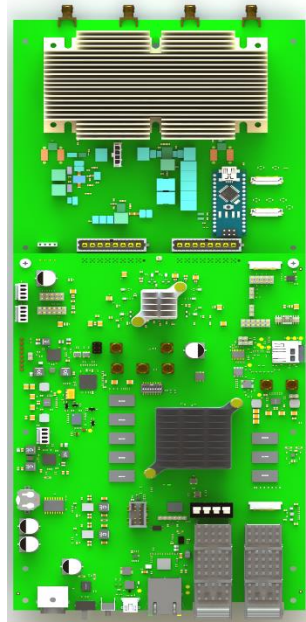
Figure 3: RFFE and ORU cards

SI/PI Simulations

Multiple simulations are run to optimize functionality and performance of each interface, thus minimizing the chances of design revision.

Stack-up is calculated by selecting the dielectric material type required to meet the signaling performance requirements. Prepreg/copper thickness as well as number of signal layers/GND/Power planes are carefully setup to meet the design requirements and keeping it cost effective. Trace width calculation is done to meet impedance requirements.

Parametric via optimization simulation is also done to design impedance controlled via for minimizing signals losses. See Figure 4.
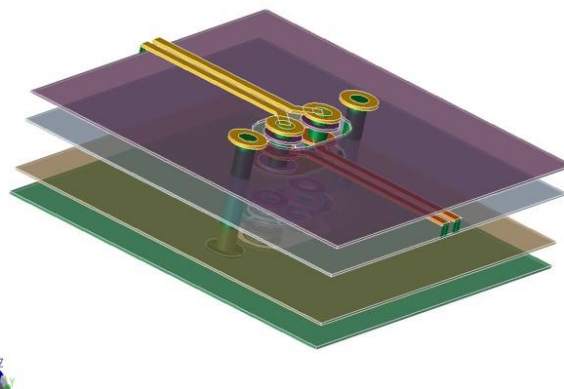

Figure 4: 3D via structure for design optimization

Critical high speed signal design rules like maximum allowed trace length are defined through several pre-layout simulations. This is the key to first time success of this design. Via stub is minimized by back drilling to reduce return loss and improve signal quality of the high-speed differential pairs as shown in Figure 5. To validate the routing rules, insertion and return loss measurements as well as serial link simulations are performed for the QSFP signals which produce eye diagrams as shown in Figure 6.
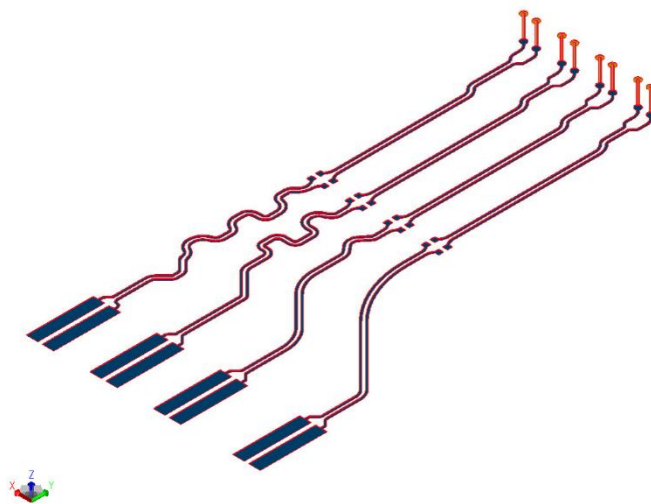

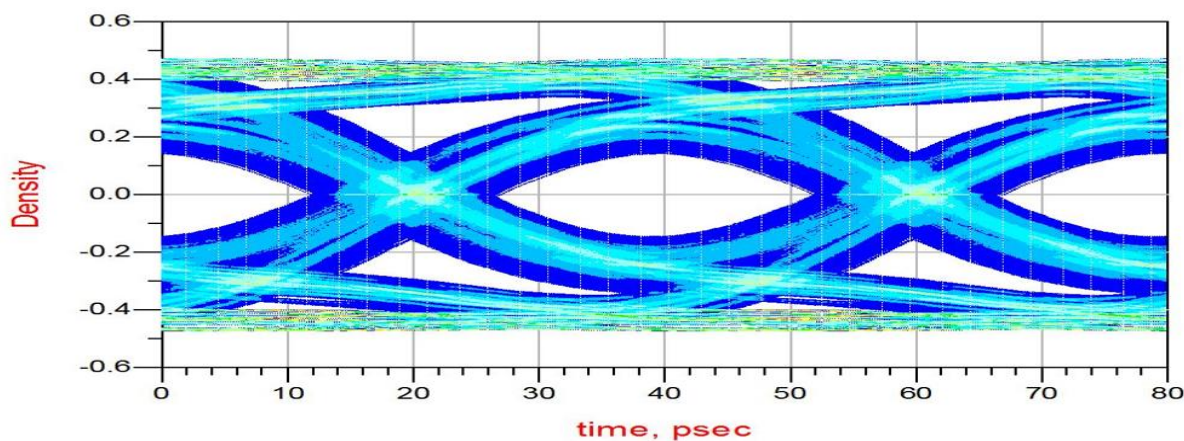Figure 5: 3D view of high speed routing

Figure 6: Eye diagram results of Serial Link Simulation

The DDR interface is demanding in terms of signal integrity and timing requirements. To ensure that the DDR interface functions properly, pre-layout simulations are run to determine routing topology and set delay matching rules. Termination resistor value selected minimizes ringing, noise and reflection. Post-layout simulation is done to get Eye, Wave and Timing/Mask results for verification that the signals are matched within required timing with less ringing and maximum eye-aperture widths.

Power is one of the main challenges faced in designing this board. Power AC simulation is done to optimize the power delivery network and reduce the cost of decoupling/bypass capacitors.

Power DC simulation is run to ensure that the IR drop is within acceptable limits for this design. Extra care is taken while selecting ferrite beads, inductor or supply regulators for critical power rails to minimize the IR drop and thermal heating issues. To make sure that the PDN circuit will work effectively, IR drop; via current; plane current density; Joule heat thermal simulations are done on all power rails. Figure 7 shows the IR drop simulation results.
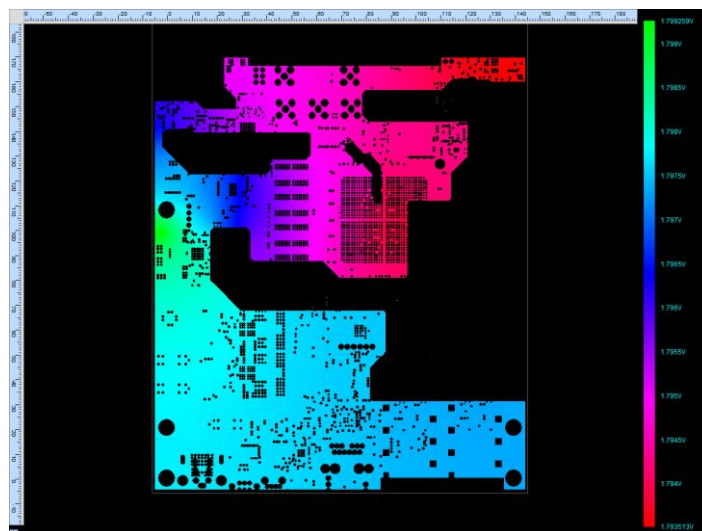

Figure 7: Power DC analysis results

Mechanical Enclosure

The mechanical board and enclosure size are designed optimally to meet the overall product design constraints and requirements. ORU card size is 9 x 6 x1.5 inches; Adapter card is 6.5 x 6 x 0.5 inches and RFFE card is 6.4 x 6 x 1.2 inches. However, the overall enclosure size specifications are 14.9 x 8 x 2.6 inches. See Figure 8.

Sheet metal for the enclosure is Aluminum alloy which is lighter and easier to manufacture as compared to other options like low carbon steel. End capsulations are of ABS plastic, which is inexpensive, lightweight, shock absorbent, and durable too.

To a great extent, off the shelf hardware selection is preferred for mechanical assembly to keep the cost low and design simplified. This includes the washers, screws, stand-offs, and other mechanical components.

There are several enclosure joining mechanisms like sliding, top/bottom joining, etc. but mating of covers with screws is preferred keeping in mind the application of the unit. Chassis shape design underwent several revisions for contour changes in order to lower the cost but retain aesthetic appeal.

Figure 8: ORU Enclosure

Thermal Analysis

ORU & RFFE cards are thermally simulated to determine critical components temperature and heat flow under certain power loads and ambient conditions. Objective is that the critical component temperatures must not exceed rated maximum temperature range.

The unit is thermal complaint for System level (inside the enclosure) as well as Module level (the Standalone PCB) as verified using a CTM (Compact Thermal Model).

Different configurations are applied for both the ORU and RFEE cards. Placement of connectors and heighted components in ORU are positioned to ensure there are no airflow blockers and temperatures are within allowed range. Different heat sinks are selected according to major heat dissipated components. As RFFE is designed after ORU, configurations for RFFE are optimized to have a new fan with more airflow but unchanged position.

As a result, all thermal model simulation results are PASS based on selected thermal solutions of heat sinks and fans having better air flow but lesser pressure noise as shown in Figure 9.
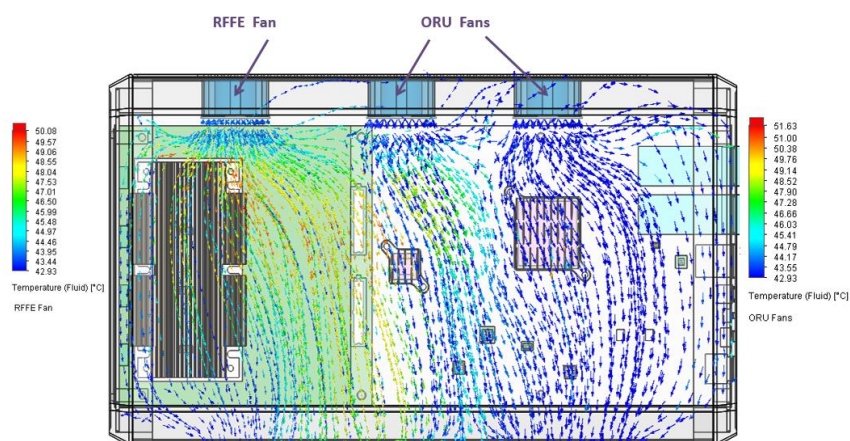
Figure 9: Thermal Analysis results

O-RU Roadmap Plan

This white paper highlights Whizz Systems contributions to the ORU white box solution. The complete O-RU is the result of combined efforts of multiple partners including Intel, ADI, Radisys and Comcores. The O-RU white box solution is available now for testing and general availability is planned for end of 2020 or early 2021. Other derivatives such as 2T2R, 8T8R or lower power versions are possible. If interested, please reach out to us.

O-RU Product Development Partners

- Intel provided Arria®10 FPGA SoC which is the central processing chip used in the design.
- Analog Devices provided both the Digital Front-End (DFE) and Radio Frequency Front-End (RFFE).
- Whizz Systems developed the hardware design from concept to physical product with major components provided by both Intel® and ADI.
- Comcores provided the FPGA Intellectual Property (IP) for O-RU function implementation on the FPGA.
- Radisys helped in integration of O-RU software with Intel® FlexRAN server

Further Reading

[1] https://www.design-reuse.com/articles/48289/opening-the-5g-radio-interface.html

[2] https://hub.radisys.com/white-papers/delivering-open-radio-unit-for-outdoor-small-cell-deployment

About Whizz Systems

Whizz Systems was founded in January 2000 and incorporated in California, USA with primary focus on electronics product design, development, manufacturing and consulting services. With over 150 in-house experts, we are equipped to successfully design and develop the products that our customers need in today's rapidly advancing market. Whizz is headquartered in heart of Silicon Valley, the hub of innovation and technology, with offices located globally. Whizz has an extensive history and successful track record of having served top-tier customers worldwide. Whether a client has small isolated needs or entire product design and development, we are here to be a partner and an extension of our clients' resources at any and every step along the journey. Moving forward, Whizz aims to be the integrated systems, hardware, software and manufacturing turnkey partner and expand its clientele world over.

Whizz Systems Support

Whizz will support derivatives of this product. If interested, please contact Muhammad Irfan at +1-408-980-0400; mirfan@whizzsystems.com

Why Whizz Systems

- Working for Top-Tier customers proves our credibility
- Highly Integrated Value Added Services
- Competent experienced team for high-end work
- Flexibility for the customer to engage at any level
- Strong presence in Silicon Valley Onshore-Offshore Resource Model to
    - Leverage cost effectiveness
    - Improve schedules
    - Scale resources

September 2020